Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of forming a capacitor in a trench etched into a silicon substrate comprising the steps of:
etching a trench to a trench depth with a trench cross section and having trench interior walls;
forming a layer of oxide on said interior walls such that the oxide has a smaller thickness in corners of said trench than on said walls;
etching said oxide until silicon on said interior walls is exposed in said corners, whereby remaining oxide remains on said interior walls adjacent to exposed silicon in said corners;
forming corner nitride on said exposed silicon in said corners;
stripping said remaining oxide from said interior walls selective to nitride;
etching said interior walls selective to nitride, thereby extending said trench cross section laterally at locations of said interior walls;
forming a capacitor dielectric on surfaces of said interior walls; and
forming a center electrode in an interior volume of said trench.

[c2] A method according to claim 1, further comprising a step of forming an etch-resistant collar in an upper portion of said trench before said step of etching said interior walls, whereby said upper portion retains said trench cross section after forming said capacitor, forming a field effect transistor in said upper portion connected between said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, thereby forming a DRAM cell.

[c3] A method according to claim 1, in which said layer of oxide on said interior walls is thermally grown.

[c4] A method according to claim 1, in which said corner nitride is thermally grown.

[c5] A method according to claim 1, in which said step of etching a trench to a trench depth is performed by first etching said trench to said collar reference depth; forming an etch - resistant collar, resistant to said step of etching said interior walls, on said interior walls above said collar reference level; and
thereafter etching said trench to said trench depth.

[c6] A method according to claim 5, further comprising a step of, after forming said capacitor, forming a field effect transistor in said upper portion connected between

said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, thereby forming a DRAM cell.

[c7] A method according to claim 5, further comprising a step of etching said oxide to remove a corner thickness of oxide, thereby exposing a corner distance of exposed silicon between each corner and said remaining oxide.

[c8] A method according to claim 1, further comprising steps of:
filling said trench with a temporary material up to a collar reference level;
forming an etch - resistant collar, resistant to said step of etching said interior walls, on said interior walls above said collar reference level; and
removing said temporary material;
said step of removing said temporary material being performed before said step of etching said interior walls, whereby said interior walls are etched only below said collar reference level.

[c9] A method according to claim 2, in which:
said steps of filling said trench with a temporary material, forming said collar and removing said temporary material are performed before said step of forming said oxide with a smaller thickness in the corners.

[c10] A method according to claim 8, further comprising a step of, after forming said capacitor, forming a field effect transistor in said upper portion connected between said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, thereby forming a DRAM cell.

[c11] A method according to claim 8, further comprising a step of etching said oxide to remove a corner thickness of oxide, thereby exposing a corner distance of exposed silicon between each corner and said remaining oxide.

[c12] A method according to claim 9, further comprising a step of, after forming said capacitor, forming a field effect transistor in said upper portion connected between said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, thereby forming a DRAM cell.

[c13] A method according to claim 9, further comprising a step of etching said oxide to remove a corner thickness of oxide, thereby exposing a corner distance of exposed silicon between each corner and said remaining oxide.

[c14] A method according to claim 1, in which:
said step of forming said oxide with thinner corners is performed before a step of filling said trench with a tem-

porary material up to a collar reference level;
said oxide is stripped above said collar reference level;
said temporary material is removed, after which;
said step of etching said oxide until silicon on said interior walls is exposed in said corners is performed;
said step of forming nitride on said exposed silicon is performed, whereby said nitride is formed in said corners below said collar reference level and simultaneously said etch - resistant collar is formed on all of said interior wall surface above said collar reference level.

[c15] A method according to claim 13, further comprising a step of, after forming said capacitor, forming a field effect transistor in said upper portion connected between said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, thereby forming a DRAM cell.

[c16] A method according to claim 13, further comprising a step of etching said oxide to remove a corner thickness of oxide, thereby exposing a corner distance of exposed silicon between each corner and said remaining oxide.

[c17] A trench structure formed in a semiconductor substrate comprising
a portion of said trench having a polygonal cross section comprising four straight main sides oriented with an an-

gular difference between consecutive main sides; four inner projecting corners disposed between said four main sides, said four inner corners being located closer to a center of said polygonal cross section than said main sides; and connecting lines connecting said inner corners with said main sides.

[c18] A capacitor formed in a trench in a semiconductor substrate comprising
a portion of said trench having a polygonal cross section comprising four straight main sides oriented with an angular difference between consecutive main sides; four inner projecting corners disposed between said four main sides, said four inner corners being located closer to a center of said polygonal cross section than said main sides; and connecting lines connecting said inner corners with said main sides;
a node dielectric disposed on interior surfaces of said lower portion of said trench; and
a conductive center electrode disposed within said trench and abutting said node dielectric.

[c19] A capacitor according to claim 18, further comprising an upper portion of said trench retaining its original cross section and a lower portion of said trench disposed within a buried plate and having said polygonal cross section.

[c20] A capacitor according to claim 18, further comprising a transistor formed within said upper portion of said trench connected between said center electrode and a first cell contact, said transistor being controlled by a gate connected to a second cell contact, said capacitor and said transistor together thereby forming a DRAM cell.